# CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Department of Electrical and Computer Engineering

# ECE 526L

LAB – 7 :

# SCALABLE MULTIPLEXER

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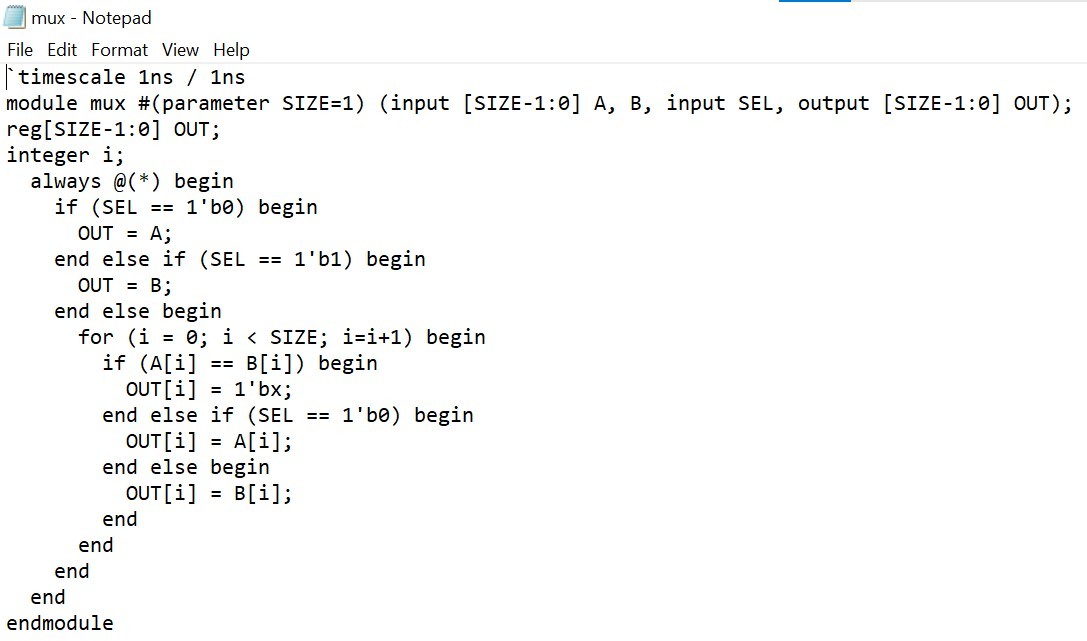
### INTRODUCTION:

In this lab we will create a Verilog model of a scalable multiplexer using Synopsys VCS in Linux OS environment and different terminal commands

### METHODOLOGY:

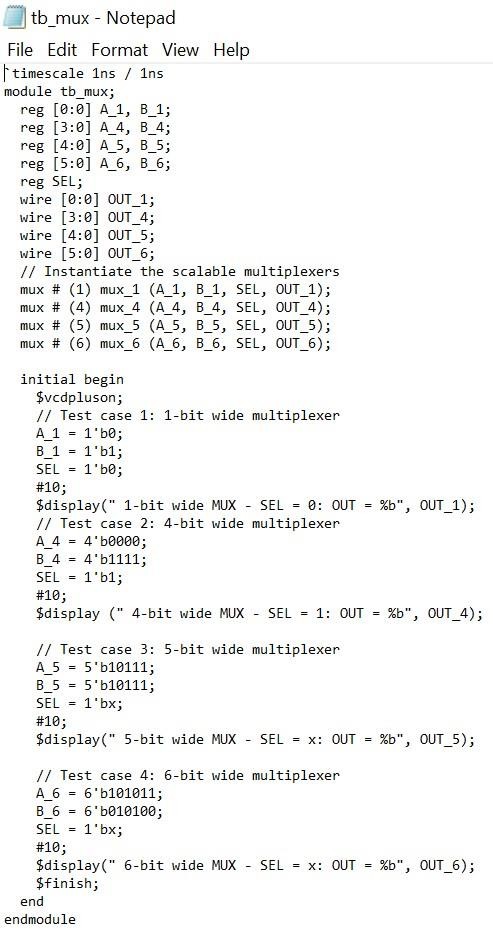
In this lab we will create a Verilog model of a scalable multiplexer using the given module and steps in assignment we should write a design code for the scalable multiplexer and save it as “ mux.v ” in a new folder named “lab7”

The module name and file name should be consistent



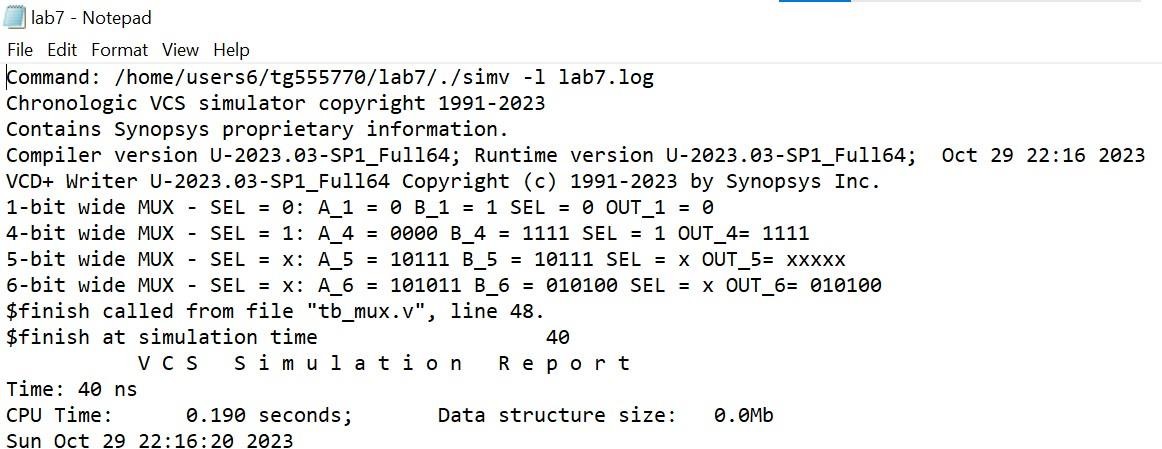
This is the fig of **Design code**

Now we should write the test bench code for the design code for that we should create four instances of scalable multiplexer by using 1,4,5,6 for different widths and consider the points given in assignment and that should be saved as **“ tb\_mux.v** ” shown in below figure.



Now compile the two files by using the command line as follows “vcs -debug\_access+all mux.v tb\_mux.v”

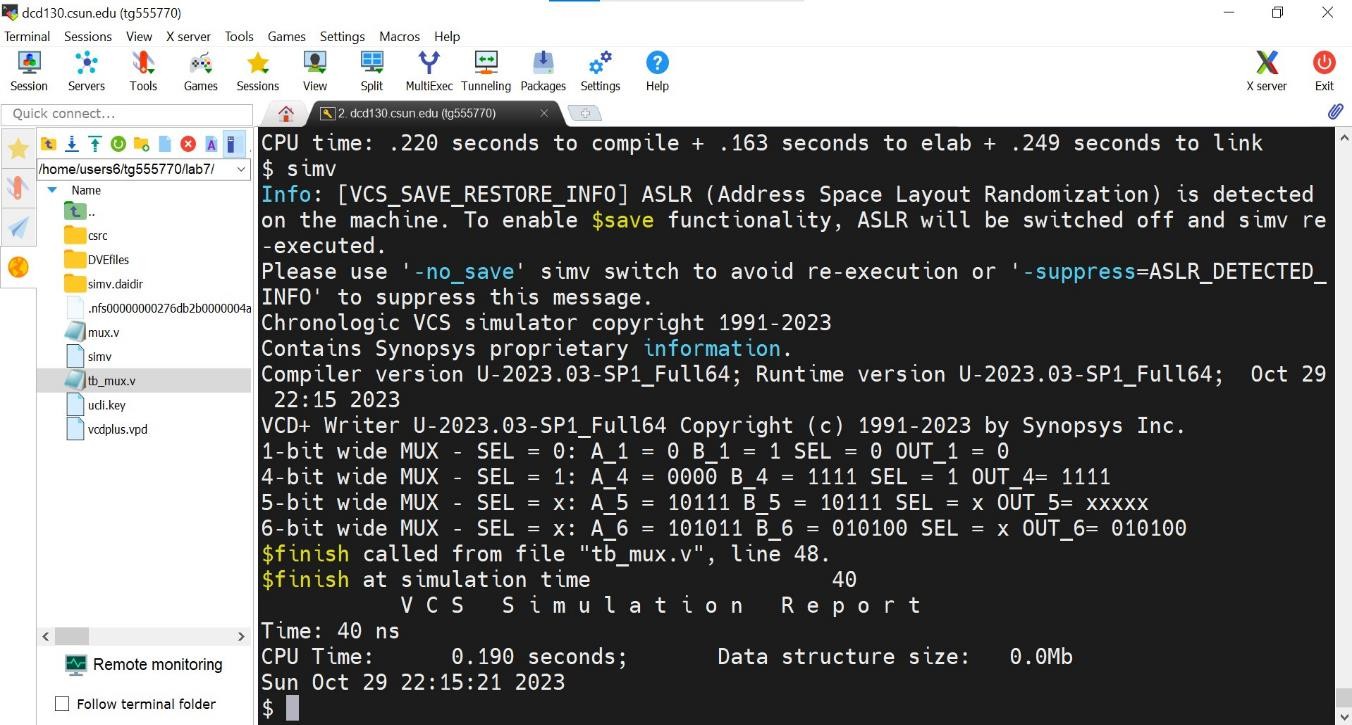
To start the simulator type simv -l lab1.log ,by using this command we will get logfile and simv outcome.



This the **Log File** which I created as shown in the above figure.

If we don’t see any error messages if everything is typed correctly then output should look like this as shown in below figure.

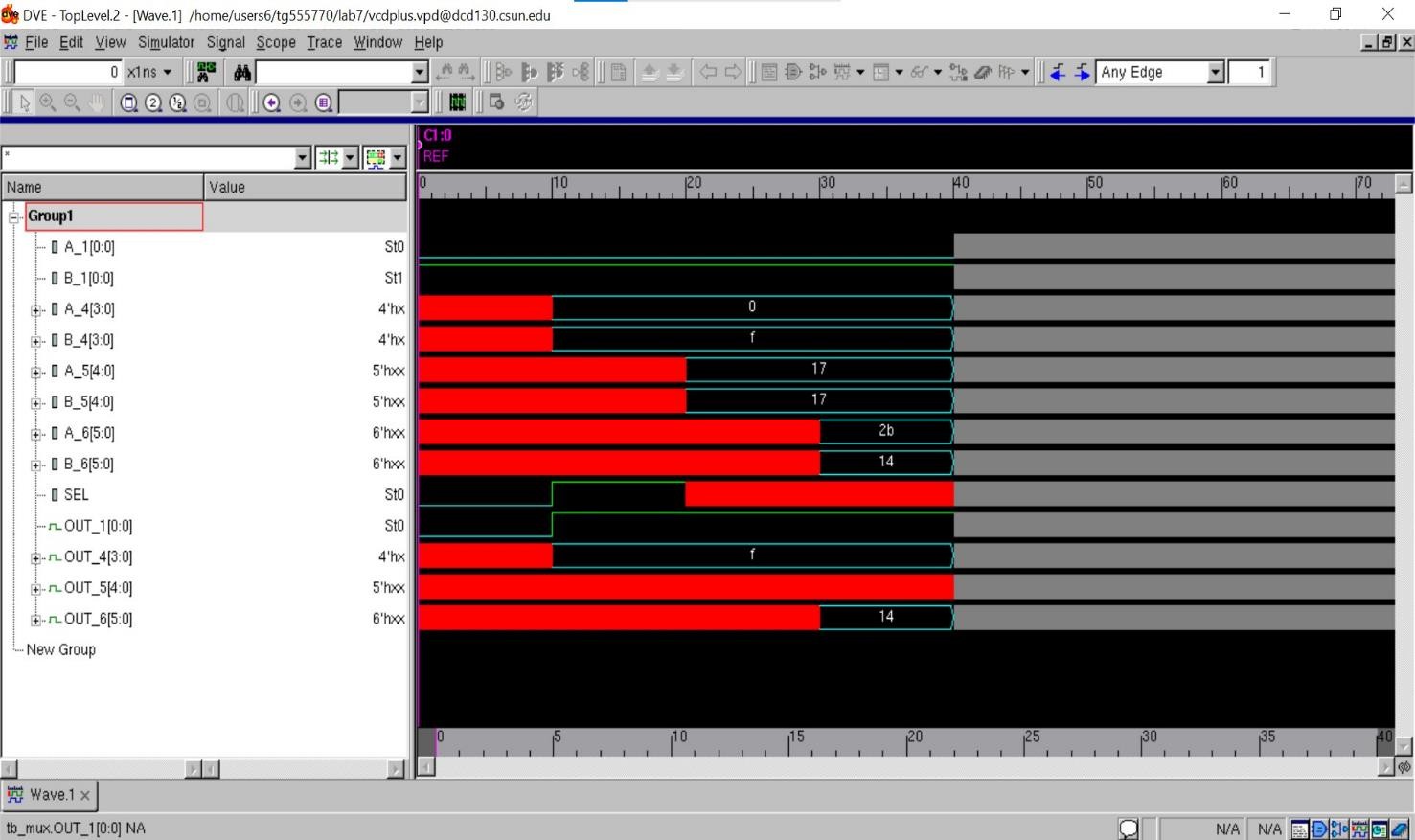
**SIMV:**



To see the waveforms we should use the software named “DVE”

To see the wave form first type “dve” command line then we will get the blank simulation window then go to file and open database then choose vcdplus.vpd and open the file.

Then finally select all the signals with the mouse ,then right click and select to “ add to wave->new wave view”. Then we will get the waveform as shown in below figure.



## Analysis of Result:

scalable multiplexer refers to a digital circuit that can select one of multiple input signals and route it to the output based on a control

signal. The result for a scalable multiplexer in Verilog is typically defined using a case statement or an if-else construct in given lab we taken 4 instances in different cases depend upon on the inputs value we provide and the sel value the output value varies. By increasing the number of input signals and utilizing the proper control signal width, we may scale this idea to construct larger multiplexers, such as 4:1, 8:1, or even larger multiplexers.

I hereby attest that this lab report is entirely my own work.I have not copied either code or text from anyone ,nor have I allowed or I will anyone to copy my work.

Name(printed) Gunupudi Tarun Kumar

Name(signed) G.Tarun

Date 10/29/2023

**Conclusions:** In this lab we simulated scalable multiplexer using synopsys Vcs in Linux OS environment and got the required waveform.